**Experiment Name:**

Design and implementation of a NOT/NAND/NOR gate.

**Design and Implementation of NOT Gate**

**Objective:**

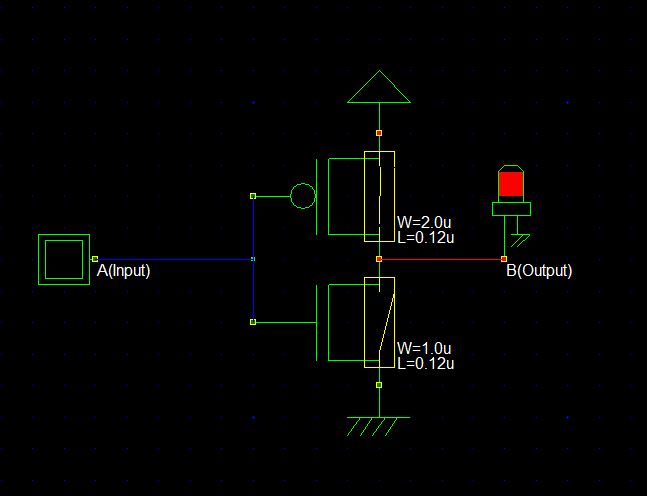
**Logic NOT Gates** are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function.

**Theory:**

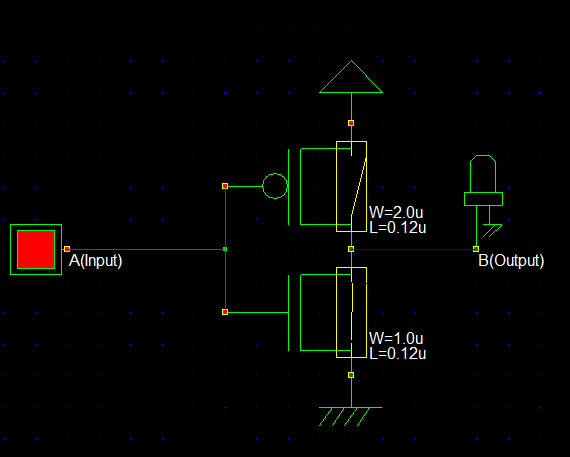
The inverter (NOT circuit) performs a basic logic function called “inversion” or “complementation”. The inverter changes one logical level toits opposite level. In terms of bits, it changes logic1 to logic 0 and logic 0 tologic1.It’s needed some nmos and pmos to connect with vdd(voltage) and gnd(ground).Then connect with source and light to find the input and output from the circuit.

**Circuit Diagram**

if input A is 0,



If input A is 1,



**Verilog File:**

// DSCH 2.6h

// 9/1/2018 7:00:33 PM

// D:\Downloads\study 4-1\VLSI\Lab\Lab1\notgate.sch

module notgate( in1,out1);

input in1;

output out1;

pmos #(17) pmos(out1,vdd,in1); // 2.0u 0.12u

nmos #(17) nmos(out1,vss,in1); // 1.0u 0.12u

endmodule

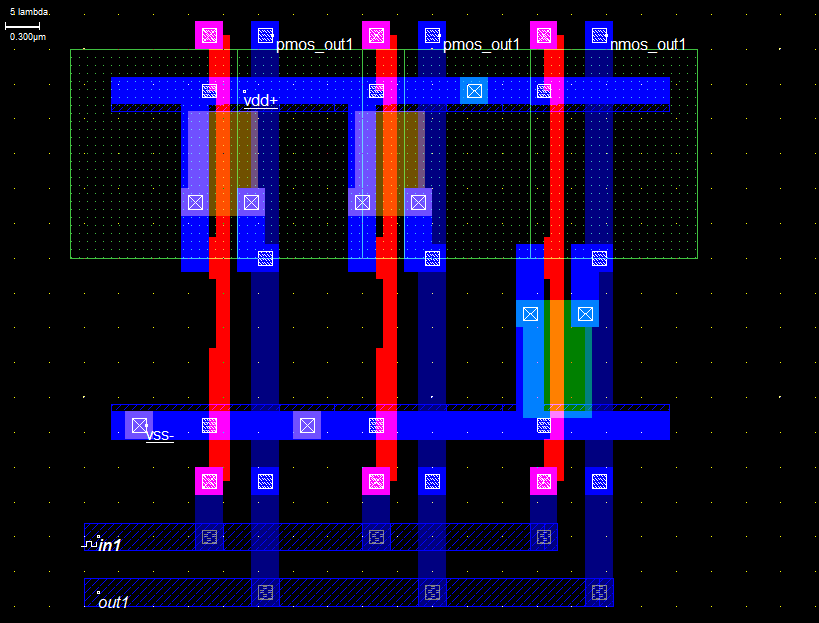
always

#1000 in1=~in1;

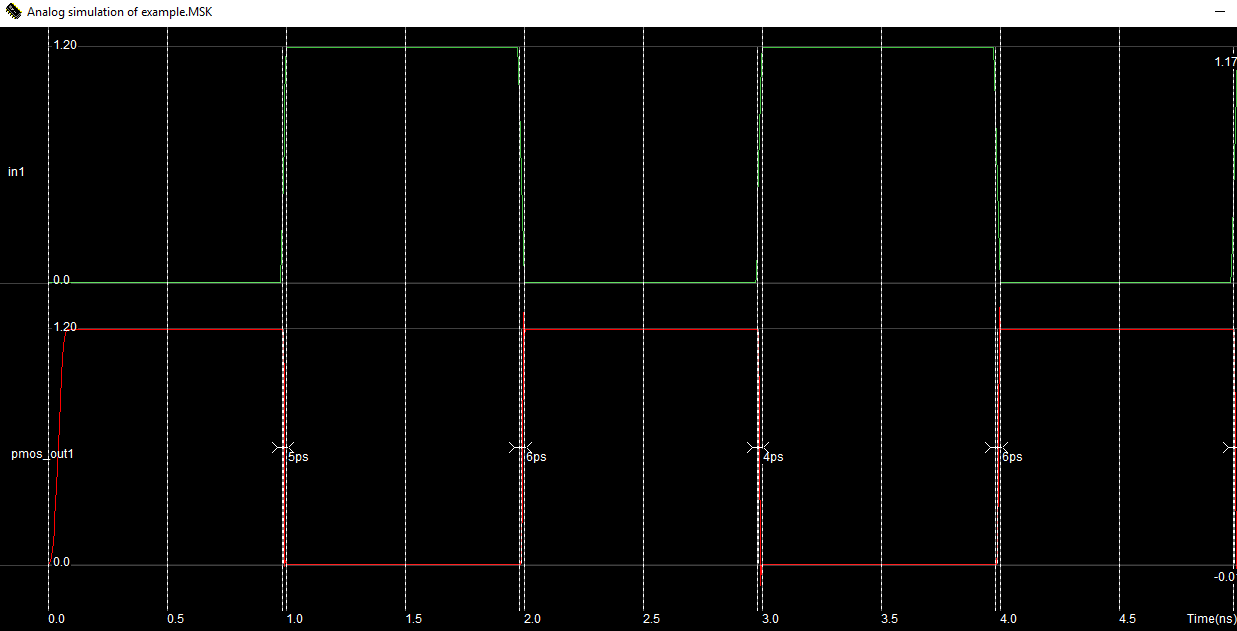
// Simulation parameters

// in1 CLK 10 10

**Layout Diagram**

****

**Timing Diagram**

****

**Discussion**

Finally we can find a timing diagram to understand and show the interaction when a primary purpose of the diagram is to reason about time. Then we can easily understand about NOT gate implementation. It can be represented by using the DSCH2 tool.

**Design and Implementation of NOR Gate**

**Objective: Logic NOR Gates** are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function.

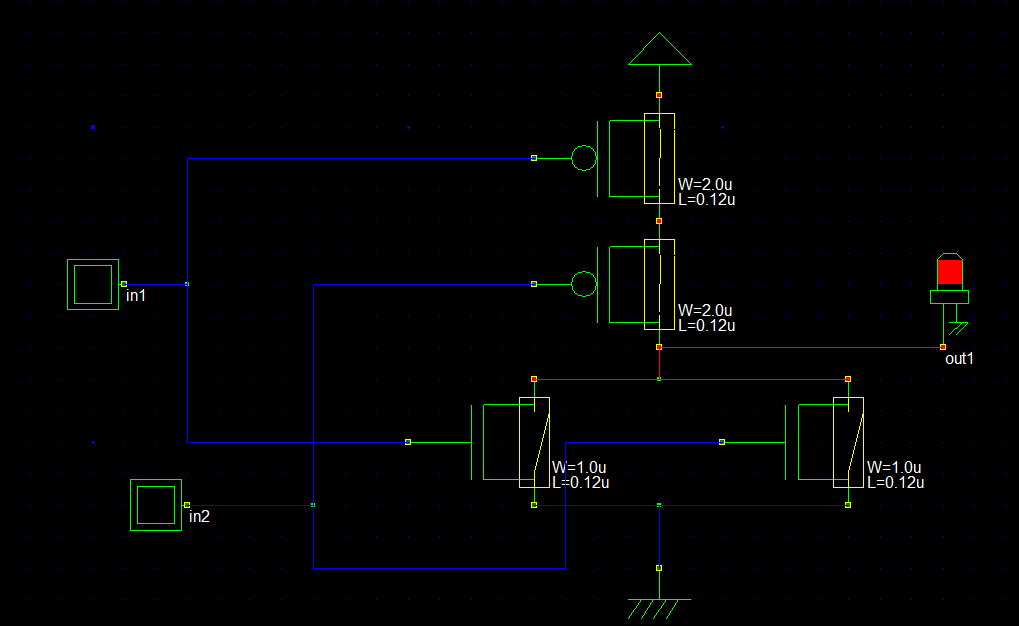
**Theory:**

The term NOR is a contraction of NOT-OR and implies an ORfunction with a complemented output. It is a universal gate. the logicaloperation of NOR gate is such that a Low output occurs when any of theinputs are HIGH. when all of the inputs are LOW, output will be HIGH.

Truth Table

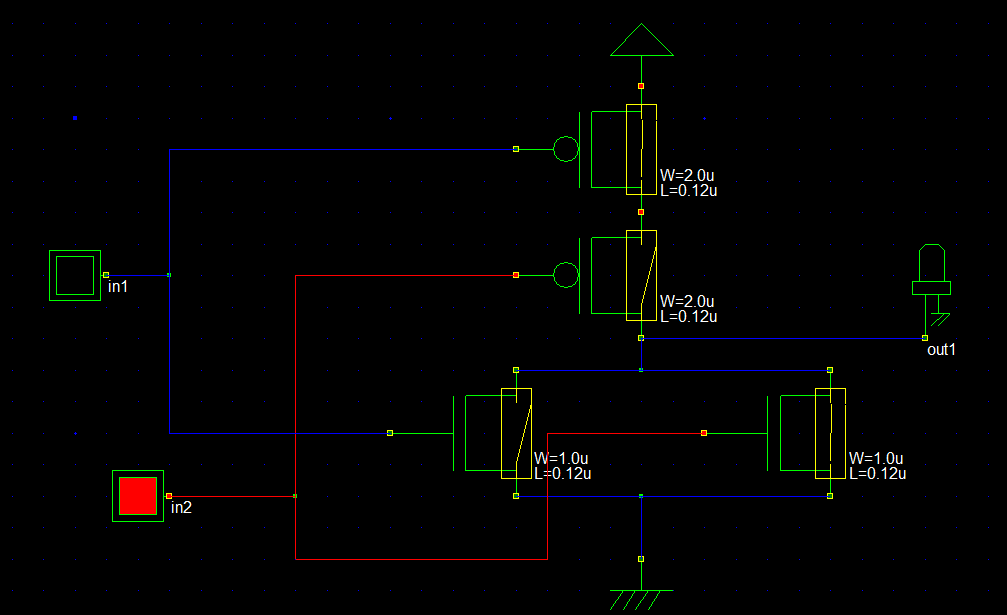
|  |  |  |
| --- | --- | --- |
| A | B | C(output) |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Circuit Diagram**

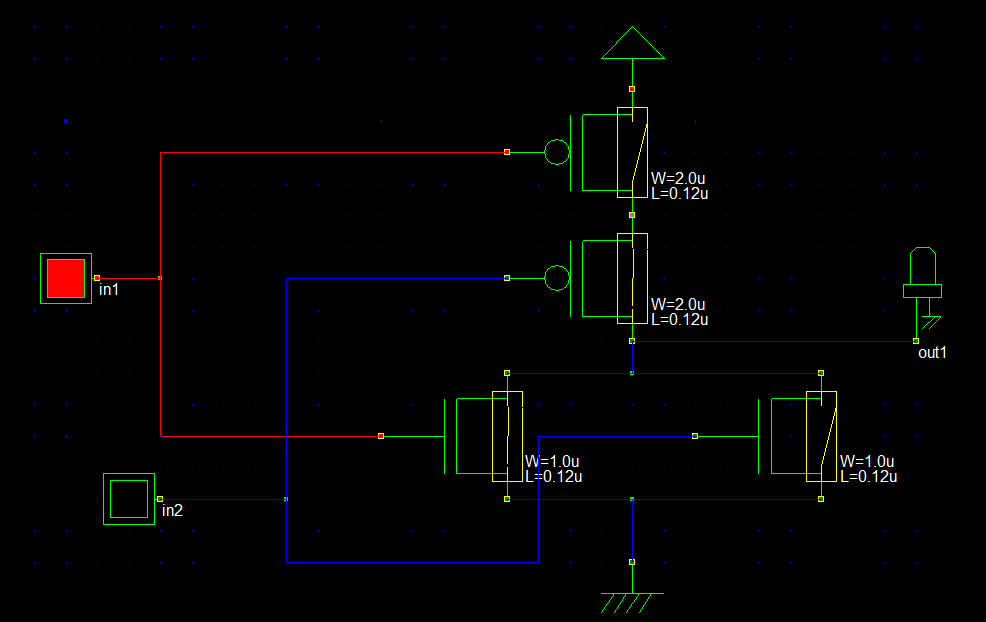
****

IF in1 and in2 is 0

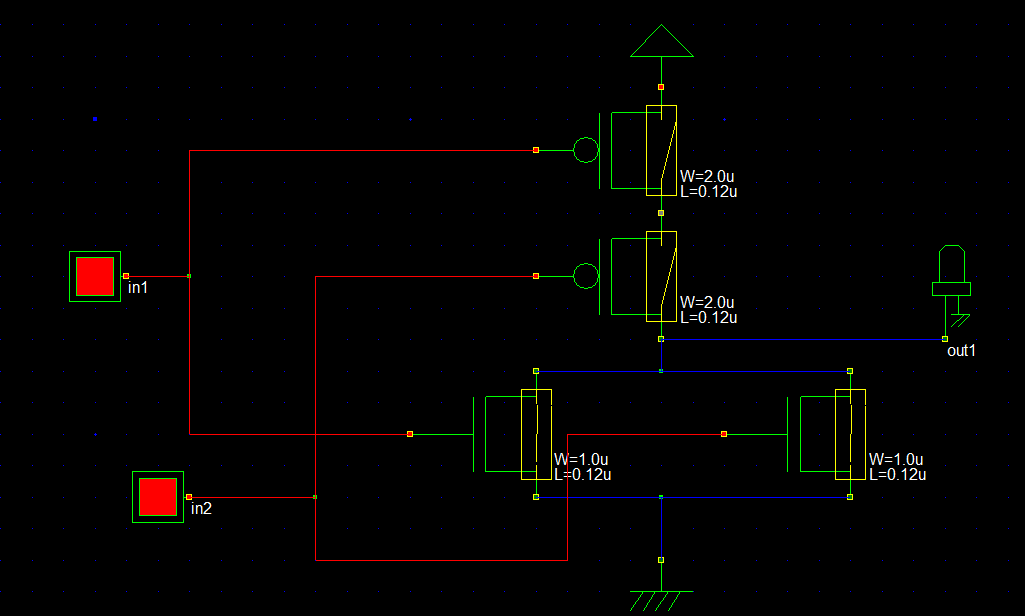
If in2 is 1 and in1 is 0,

****

If in1 is 1 and in2 is 0 ,

****

If in1 and in2 is 1 then

****

**Verilog File:**

// DSCH 2.6h

// 8/29/2018 7:00:50 PM

// D:\Downloads\study 4-1\VLSI\Lab\Lab1\norgate.sch

module norgate( in1,in2,out1);

input in1,in2;

output out1;

pmos #(10) pmos(w2,vdd,in1); // 2.0u 0.12u

pmos #(24) pmos(out1,w2,in2); // 2.0u 0.12u

nmos #(24) nmos(out1,vss,in1); // 1.0u 0.12u

nmos #(24) nmos(out1,vss,in2); // 1.0u 0.12u

endmodule

// Simulation parameters in Verilog Format

always

#1000 in1=~in1;

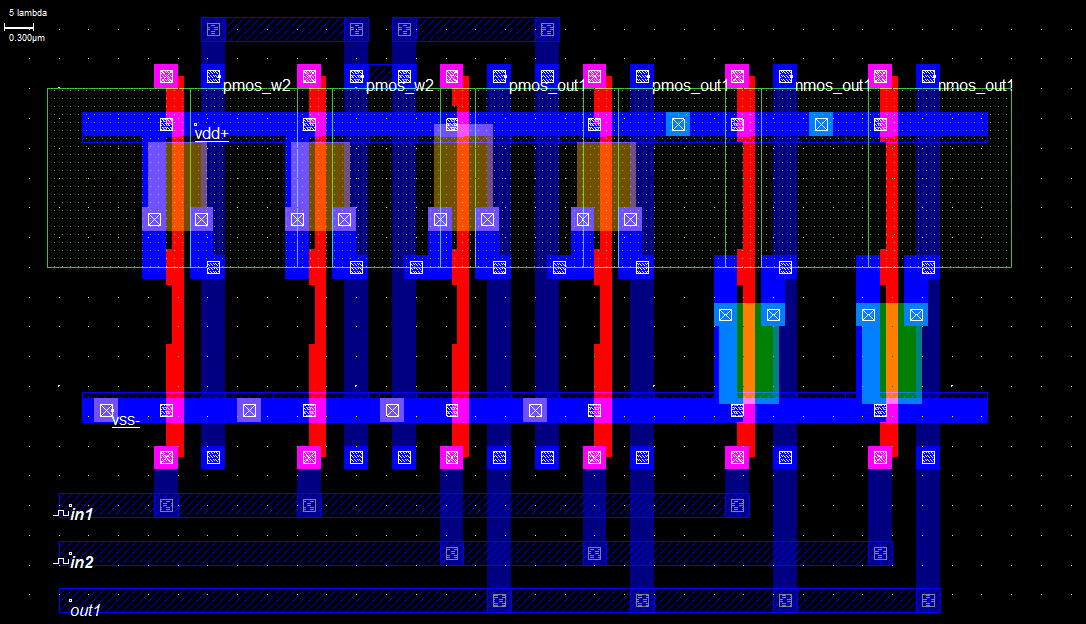
#2000 in2=~in2;

// Simulation parameters

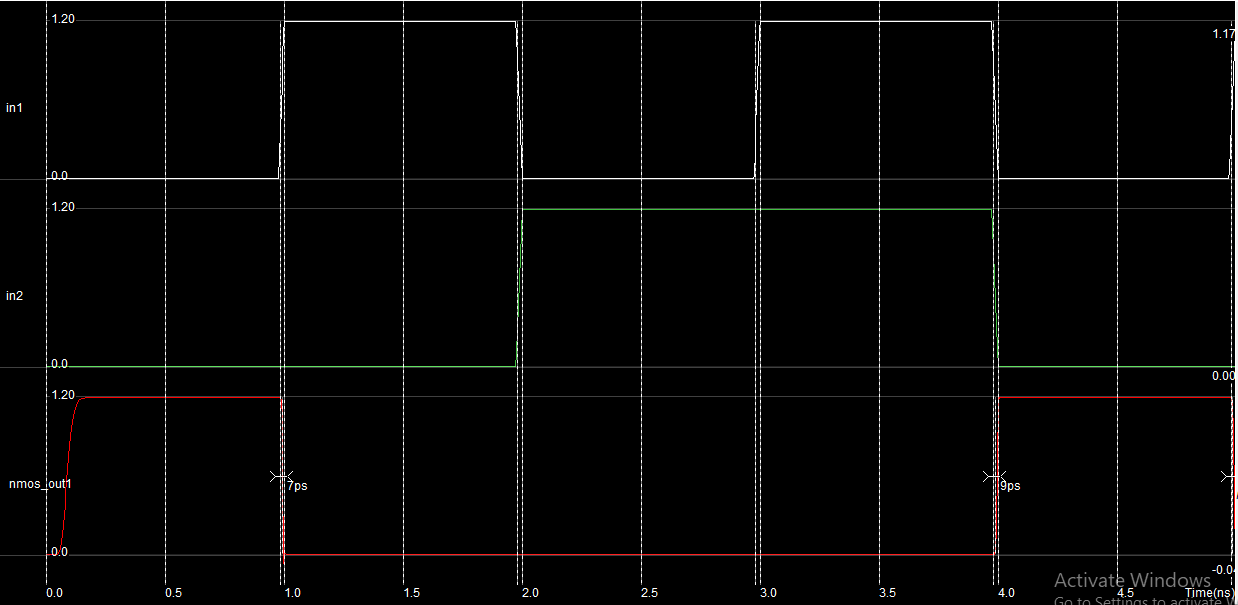
// in1 CLK 10 10

// in2 CLK 20 20

**Layout Diagram:**

****

**Timing Diagram**

****

**Discussion**

From NOR gate implementation we can easily understand this gate specification and objectives. It can also understand about circuit to define the gate implementation.

**Design and Implementation of NAND Gate**

**Objective:**

**Logic NAND Gates** are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function.

**Theory:**

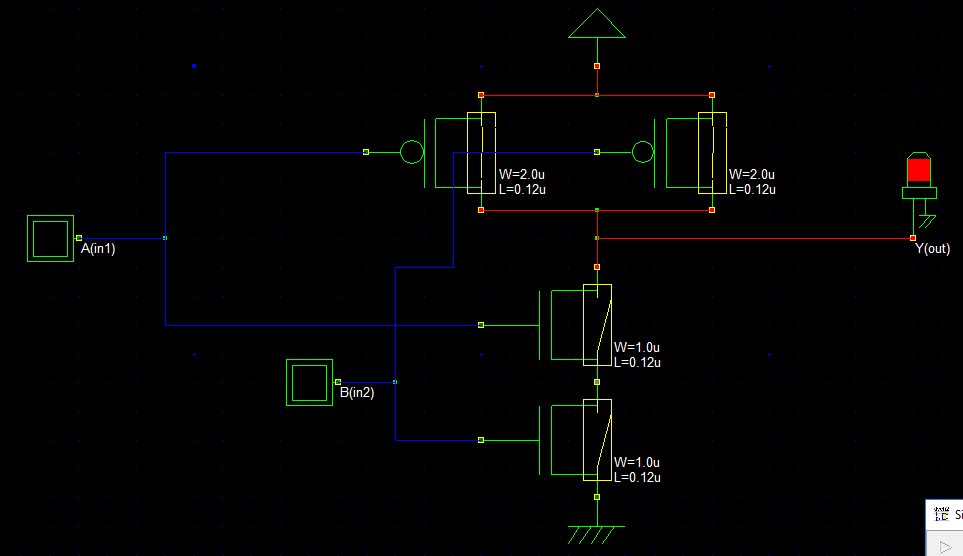
The objective of this experiment is to learn the design and simulation of CMOS schematiccircuits and to get familiar with the Automatic Layout Generation Process.

Truth Table

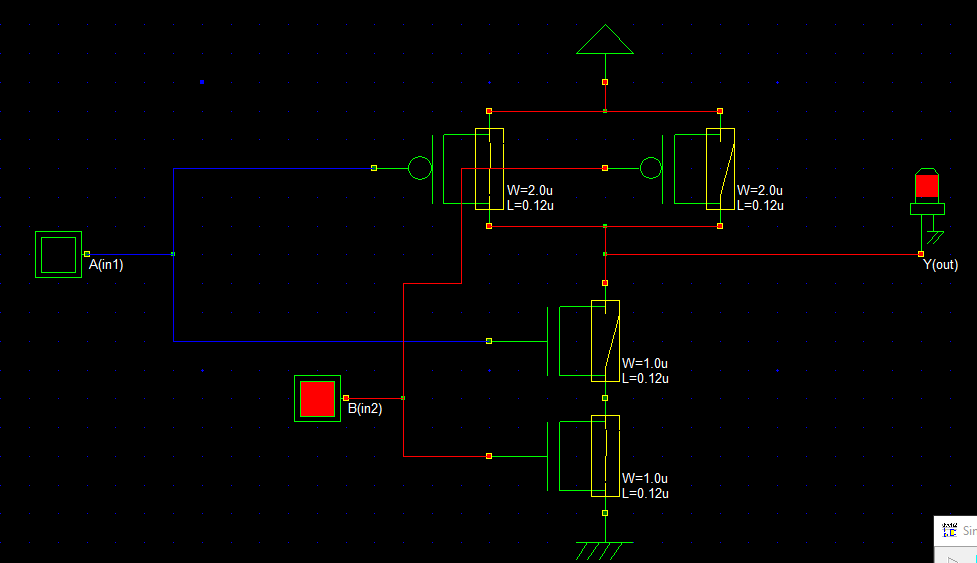
|  |  |  |
| --- | --- | --- |
| A | B | C(output) |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Circuit Diagram**

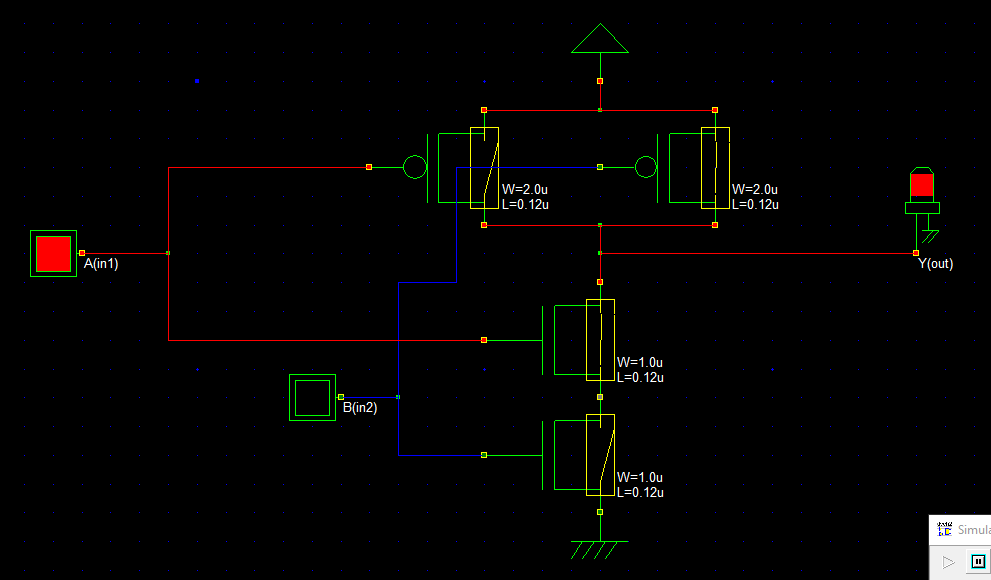
If A and B is 0,

****

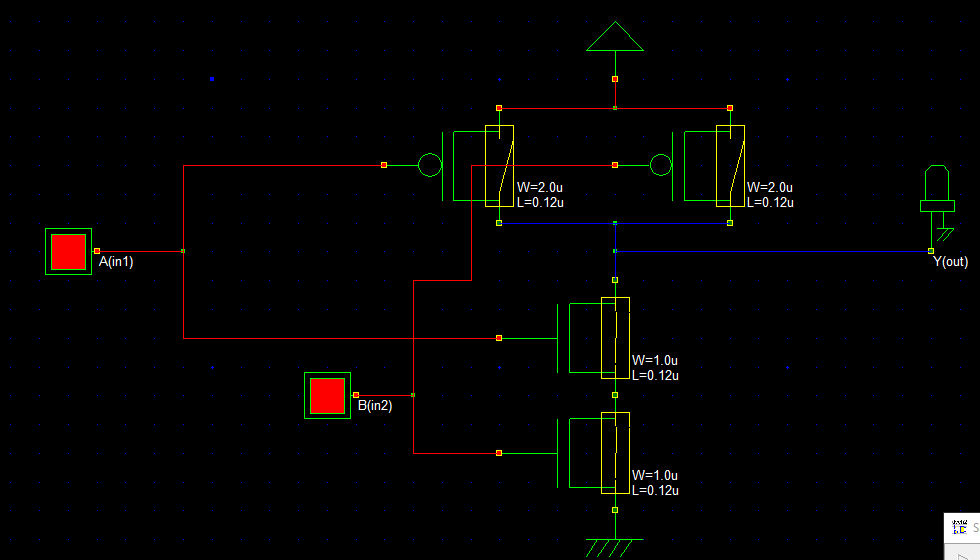
If A is 0 and B is 1,then

****

If A is 1 and B is 0, then

****

If A and B is on,then output is off

****

**Verilog File:**

// DSCH 2.6h

// 8/29/2018 8:01:00 PM

// D:\Downloads\study 4-1\VLSI\Lab\Lab1\nandgate.sch

module nandgate( in1,in2,out2);

input in1,in2;

output out2;

pmos #(24) pmos(out2,vdd,in1); // 2.0u 0.12u

pmos #(24) pmos(out2,vdd,in2); // 2.0u 0.12u

nmos #(10) nmos(w4,vss,in2); // 1.0u 0.12u

nmos #(24) nmos(out2,w4,in1); // 1.0u 0.12u

endmodule

// Simulation parameters in Verilog Format

always

#1000 in1=~in1;

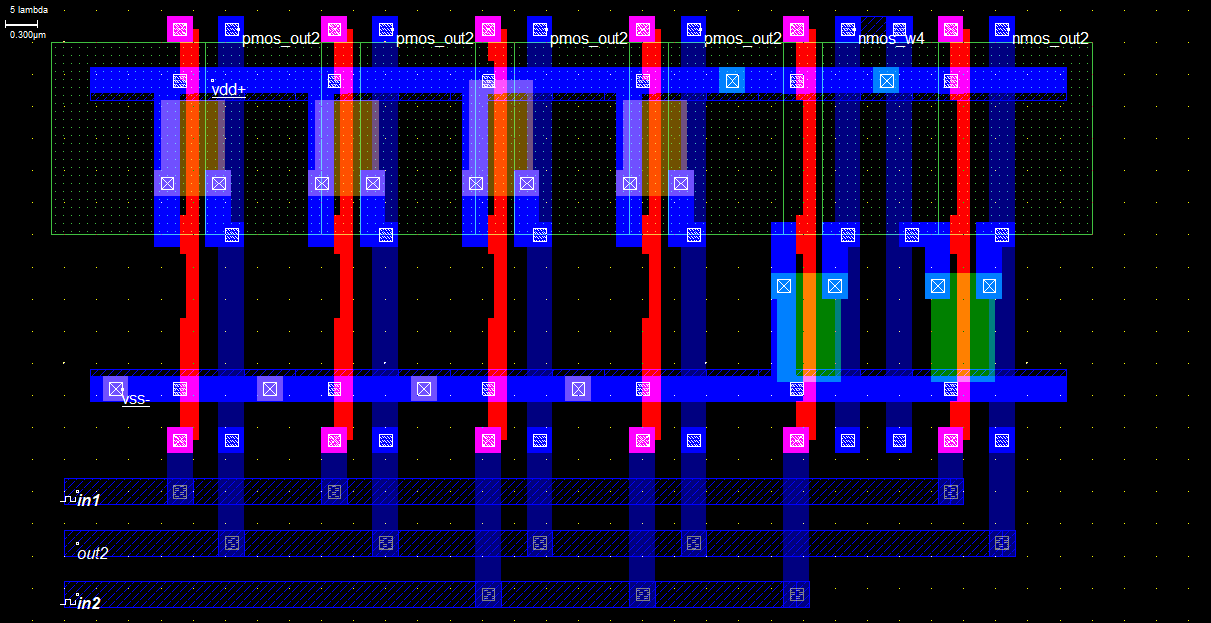
#2000 in2=~in2;

// Simulation parameters

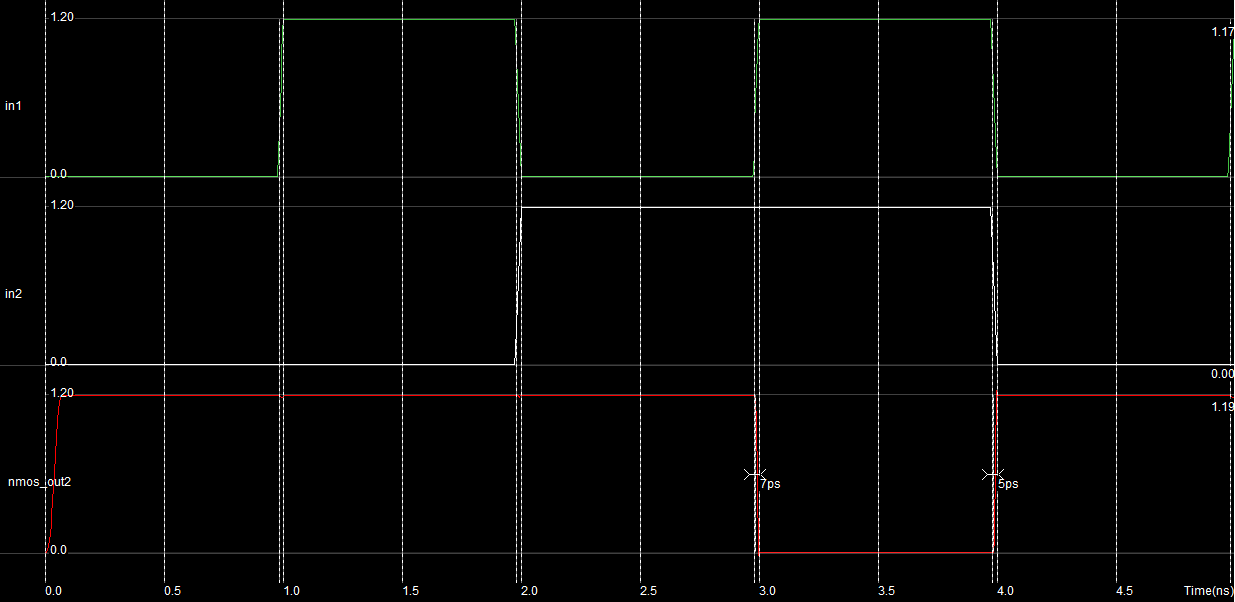
// in1 CLK 10 10

// in2 CLK 20 20

**Layout Diagram**

****

**Timing Diagram**

****

**Discussion**

It can easily connect with the system and implement the NAND gate. It can specify the system to define the value of the system and connect with the different I/O signal of the system.

**Design and Implementation of NOT Gate**

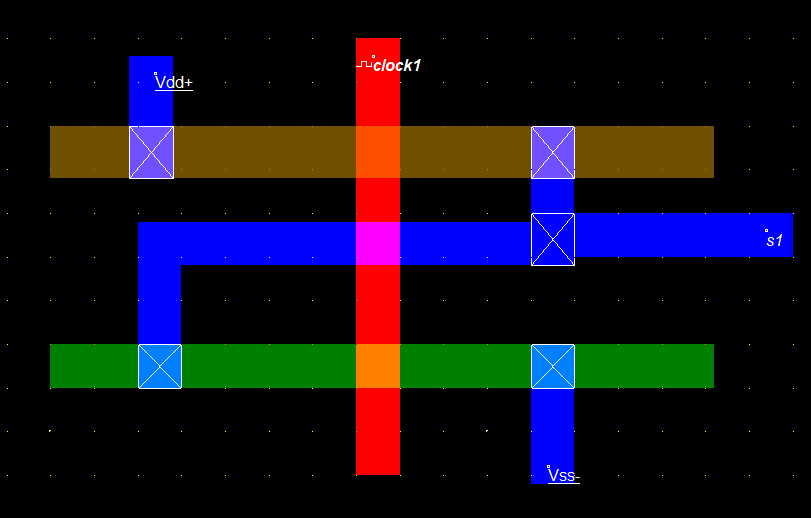
**Objective:**

**Logic NOT Gates** are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function.

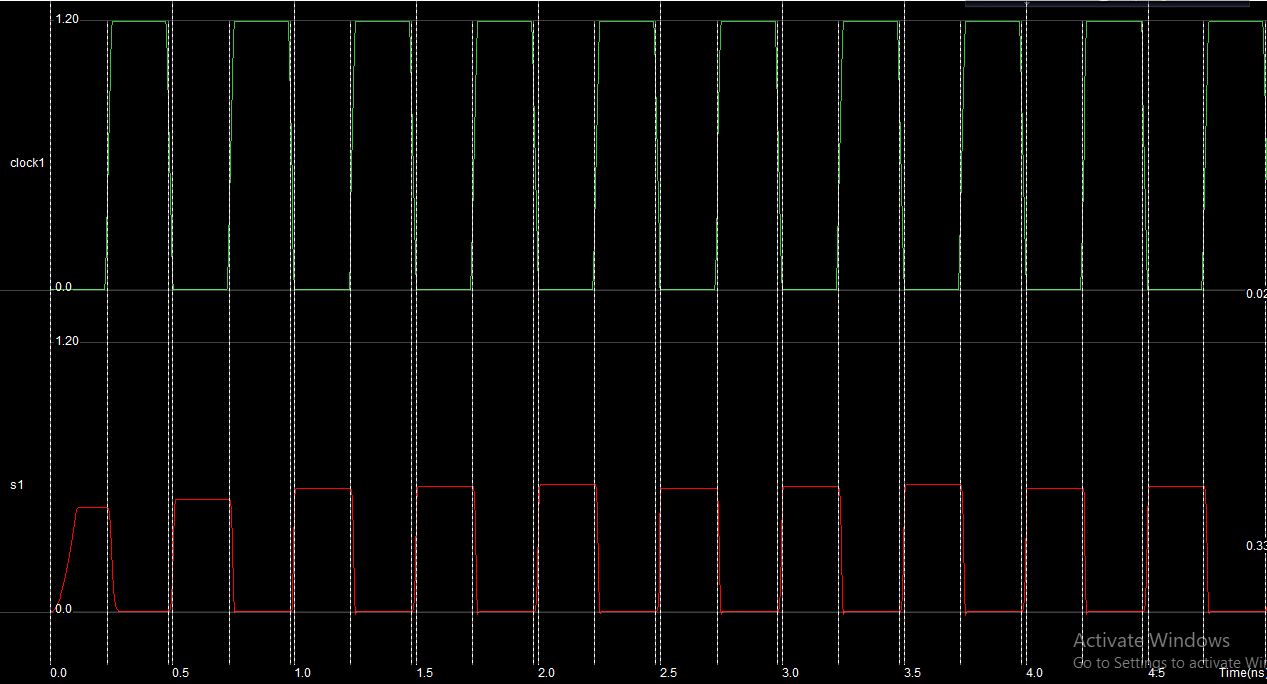
**Theory:**

For implementation of NOR gate using the stick diagram, need some n+ and p+ diffusion and then connect with the Polysilicon stick. It may define with start point of vdd and end with the s1 point. It may supply the signal with the clock pulse.

**Stick Diagram:**

****

**Timing Diagram:**



**Discussion:**

It may define the system correctly with the using of stick diagram and find the timing diagram to represent the output perfectly.

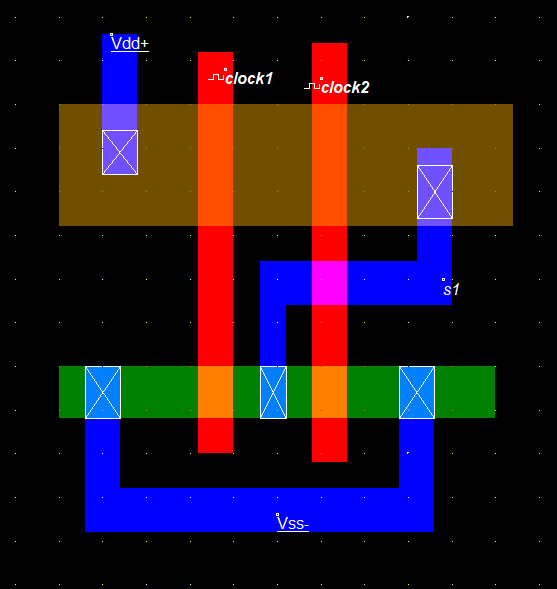
**Design and Implementation of NOR Gate**

**Objective:**

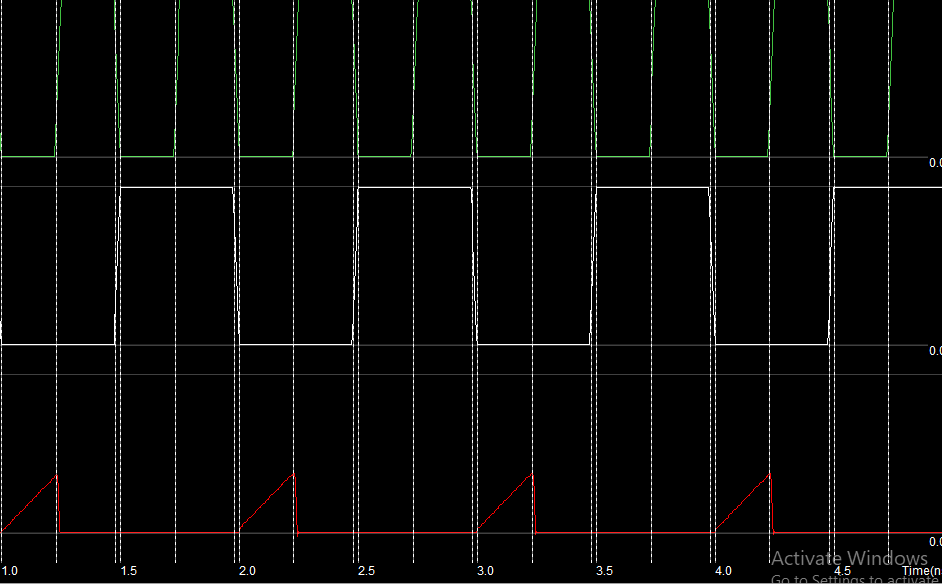
**Logic NOT Gates** are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function.

**Theory** Using two polysilicon with the take input of A and B. Then use the p+ diffusion PMOS and n+ diffusion of NMOS. For the same input of 1 then find the output of 0. Otherwise, it will be all in 0 output.

**Stick Diagram:**

****

**Timing Diagram:**

****

**Discussion:**

We can easily find the output onto the timing diagram and easily implement the signal for the using of NOR gate.

**Design and Implementation of NAND Gate**

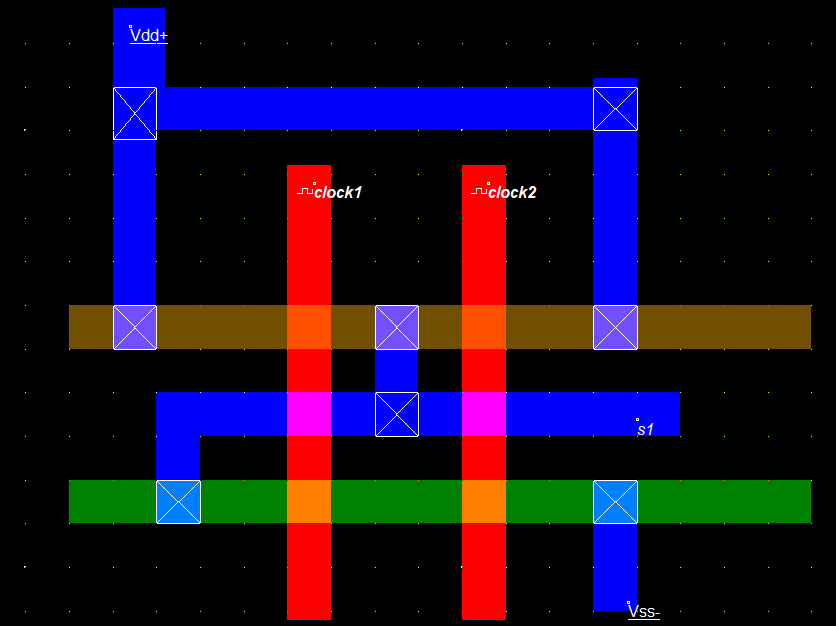
**Objective:**

**Logic NOT Gates** are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function.

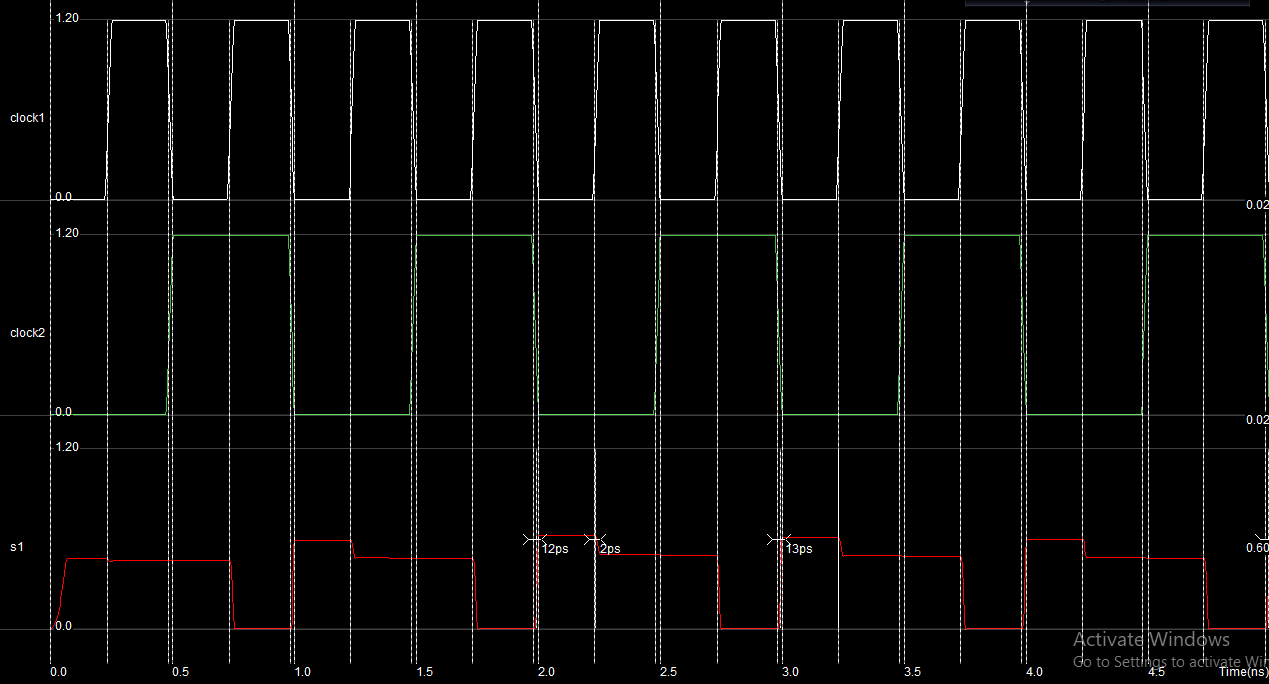
**Theory:**

Using two polysilicon with the take input of A and B. Then use the p+ diffusion PMOS and n+ diffusion of NMOS. For the same input of 1 then find the output of 1. Otherwise, it will be all in 0 output.

**Stick Diagram:**

****

**Timing Diagram:**

****

**Discussion:**

We can easily find the output onto the timing diagram and easily implement the signal for the using of NAND gate.